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(54) Title of the Invention: THIN FILM WIRING

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### Specification

#### 1. Title of the Invention:

THIN FILM WIRING

#### 2. Scope of Claims

(1) A thin film wiring characterized by comprising:

a transparent conductive film comprising at least one of Sn and In, and a first conductive thin film containing at least Al as its main constituent are formed on the same surface,

wherein the transparent conductive thin film and the first conductive thin film are provided through a second conductive thin film containing a high-melting point metal such as Mo, Cr, Ta, Ti, Ni, W and Pt, or an alloy, silicide, or nitride containing at least one of the high-melting point metal, and

wherein a third conductive thin film having a positive standard potential with respect to a standard potential of the first conductive thin film is formed on the first conductive thin film.

(2) A thin film wiring according to claim 1, wherein the third conductive thin film contains a high-melting point metal such as Mo, Cr, Ta, Ti, Ni, W, or an alloy, silicide or nitride containing at least one of the high-melting point metals.

### 3. Detailed Description of the Invention

#### Industrial Applicability

The present invention relates to a structure of a thin film wiring. In particular, the present invention relates to a structure of a thin film wiring of a transparent conductive film and an aluminum film.

#### Prior Arts

Conventionally, in an active matrix type liquid crystal display which uses an imaging plate or TFT (thin film transistor) array, a thin film material such as Cr, Ta, Mo, Ti, etc., and its alloy was used as a wiring material in view of processes or reliability. However, a device constituted by the wiring material had a limitation to high density, large area, and high speed operation due to the resistance value of the wiring resistance. Therefore, an aluminum film, which was widely used in semiconductor devices as a low resistance wiring material, was thought to realize the high density, large area, and high speed operation. But when the aluminum film as the low resistance wiring material is formed on a surface of or at the same surface of ITO (Indium-Tin-Oxide), it is known that a local electric field effect called pitting corrosion reaction occurs, so that pinholes are formed in the aluminum film and a favorable pattern cannot be formed. The mechanism of the pitting corrosion depends on a standard potential, and it occurs even when immersed into ultra pure water in a combination of materials which have a large difference of the standard potential such as 1.66 V for aluminum, and -0.19 V for ITO.

In order to solve this problem, a structure shown in Fig. 2 was suggested (see 19p-ZB-2 of lecture book of 48th Japan Society of Applied Physics, 1987). Thus, an ITO thin film 22 is provided on an insulating substrate 21, and after patterning it, an aluminum thin film 23 and a molybdenum thin film 24 are continuously vapor deposited. It is reported that the above structure could prevent the pitting corrosion reaction and form a favorable pattern by providing the molybdenum thin film 24, which has a parallel standard potential with the ITO thin film 22, on the aluminum thin film 23. In fact, the standard potential of the molybdenum thin film 24 is -0.2 V, which is almost the same as -0.19 V of the ITO thin film 22.

### Problem(s) to be Solved by the Invention

Thin film wirings which are applied to an imaging plate, TFT array and so forth, have to be reasonable materials in view of process margins such as chemical resistance, heat resistance, etc. For example, more than 300 °C is usually required to form silicon nitride, which is used as a gate insulating film in forming an amorphous Si (hereinafter abbreviated a-Si) TFT array by plasma CVD. In this case, since the aluminum thin film reduces the ITO thin film, and aluminum oxide is formed at an interface between the aluminum thin film and the ITO thin film, there was a problem that a favorable electrical contact between them could not be obtained.

The object of the present invention is to solve the problems of the conventional art.

### Means for Solving the Problem(s)

A structure of the present invention has a transparent conductive film comprising at least one of Sn and In, and a first conductive thin film containing at least Al as its main constituent are formed on the same surface, wherein the transparent conductive thin film and the first conductive thin film are provided through a second conductive thin film containing a high-melting point metal such as Mo, Cr, Ta, Ti, Ni, W and Pt, or an alloy, silicide, or nitride containing at least one of the high-melting point metal, and wherein a third conductive thin film having a positive standard potential with respect to a standard potential of the first conductive thin film is formed on the first conductive thin film.

### Operations

As shown above, the second conductive thin film material of the high-melting point metals such as Mo, Cr, Ta, Ti, Ni, W, etc., alloy, silicide, or nitride containing at least one of the high-melting point metals, which is formed at an interface between the aluminum thin film and the ITO thin film, does not diffuse into the ITO thin film at a temperature of 400 °C or less, electrically holds an ohmic contact, and third conductive thin film, which has a positive standard potential with respect to that of the aluminum thin film, is formed on the aluminum thin film. Accordingly, a favorable wiring pattern can be formed.

### Embodiments

An embodiment of a thin film wiring by the present invention is explained referring to Fig. 1.

For example, a patterned ITO thin film 12 with a thickness of 100 nm after a vacuum deposition is formed on an insulating substrate 11, and a chromium film 14 with a thickness of 30 nm as second conductive film, an aluminum film 13 with a thickness of 100 nm as first conductive thin film a tantalum film 15 with a thickness of 30 nm as third conductive thin film, are continuously deposited by DC sputtering. In this structure, a pitting corrosion reaction was not found by a brush cleaning with ultrapure water, and by a cleaning with fuming nitric acid. Therefore, a favorable cleaning can be achieved. Subsequently, an etching mask is formed by a photoresist, the tantalum thin film 15 is etched by oxalic acid series, the aluminum thin film 13 is etched by phosphoric-nitric acid series, and the chromium film is etched by cerium oxalate series. And a favorable aluminum wiring pattern can be obtained by removing the resist mask by fuming nitric acid. Even after a TaO thin film with a thickness of 200 nm is deposited, and a SiN thin film with a thickness of 200 nm is deposited by CVD at a substrate temperature of 350 °C, it was confirmed that an ohmic contact between the ITO thin film 12 and the aluminum wiring of the three-layer structure, i.e. an ohmic contact between the ITO thin film 12 and the chromium thin film 14 was favorable.

Although the ITO thin film has been referred to as a transparent conductive oxide film, the transparent conductive oxide film has a negative standard potential of around 1 V with respect to the aluminum thin film as long as it contains Sn or In. Therefore, the transparent conductive oxide film is not limited to the ITO thin film, but includes SnO<sub>2</sub> and so forth in the present invention as well.

Further, although the aluminum thin film has been referred to as the first conductive thin film, the first conductive thin film may be an aluminum alloy if it can obtain a low resistance, and Al-Si series, Al-Cu series, Al-Si-Cu series, are also included in the present invention.

Although the chromium film has been referred to as the second conductive thin film in the above embodiment, a favorable ohmic contact can be obtained as long as it is a high melting point material with small diffusional solid layer reaction with the ITO thin film since there is no formation of an insulating layer at an interface between the ITO thin film and the second conductive thin film. Thus, high melting point materials such as Mo, Cr,

Ta, Ti, Ni, W, or an alloy containing at least one of the high melting point materials such as NiCr, MoTa, or a silicide such as MoSi, TaSi, TiSi, NiS, WSi, or a nitride such as TiN, are also included in the present invention.

Further, although the tantalum film has been referred to as the third conductive thin film in the above embodiment, it may be a conductive thin film having a positive standard potential with respect to the aluminum thin film, not limited to the tantalum film. Therefore, a metal material such as Mo, Cr, Ti, Ni, W, or alloy of the metal material such as NiCr, MoTa, a silicide such as MoSi, TaSi, TiSi, NiS, WSi, or a conductive nitride such as TiN, are also included in the present invention.

#### Effect of the Invention

As it is clear from the above explanation, the thin film wiring of the present invention uses a high melting point material as a diffusion prevention layer for the ITO thin film and the aluminum thin film in a structure that the ITO thin film and the aluminum thin film are formed on the same surface, and a thin film material having a high standard potential on a surface of the aluminum thin film so as to prevent the pitting corrosion reaction, so that pattern formation is possible, and an ohmic contact can be held even in processes of 400 °C or less. Accordingly, the present invention has a great effect to the high speed operation and to large area substrate of a liquid crystal display device using an imaging plate or a TFT array.

#### 4. Brief Description of the Drawings

FIG. 1 shows a cross section of a main portion of the thin film wiring structure concerning an embodiment of the present invention.

FIG. 2 shows a cross section of a main portion of the conventional thin film wiring structure.

11...insulating substrate, 12...transparent electrode, 13...first conductive thin film, 14...second conductive thin film, 15...third conductive thin film

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**Liquid crystal electro-optical device for LCD or liquid crystal projector**

**- has protection circuits of TFT pairs connected to resistive dividers, each divider providing voltage set levels for one direction of overvoltage application**

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Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 4295826	A	19921020	JP 9184653	A	19910325	199248 B
US 5585949	A	19961217	US 92858148	A	19920324	199705
			US 93102956	A	19930806	
			US 94334383	A	19941103	
JP 3071851	B2	20000731	JP 9184653	A	19910325	200041

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JP 4295826	A	13	G02F-001/136	
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JP 3071851	B2	14	G02F-001/1368	Previous Publ. patent JP 4295826

Abstract (Basic): US 5585949 A

The device includes a pair of signal lines in matrix form on a substrate, several pixel electrodes formed on the substrate, and at least one TFT disposed at each pixel electrode. Also provided is a protective circuit having zener diode characteristics connected to a signal source, e.g. the TFT gate signal line or the drain/source signal line. The protective circuit protects the TFT against overvoltages emanating from the signal source, and it has two protective TFTs, each with additional respective resistive voltage dividers having two resistances.

The drain of one protective TFT is connected to a terminal other than the two signal lines while the drain of the other is connected to the signal source. The protective TFT sources are respectively connected through one resistance of their respective dividers to the signal source and the terminal respectively, as are their respective gates through their respective second resistances. The values of the first and second resistances of the voltage dividers are selected to provide a current diverting operation of these protective TFTs at

predetermined overvoltage levels.

**ADVANTAGE** - Excessive high voltage, e.g. due to static, may be quickly removed to pixel driving TFT from being subjected to damage caused by surge of current.

Dwg.6c/15

**Title Terms:** LIQUID; CRYSTAL; ELECTRO-OPTICAL; DEVICE; LCD; LIQUID; CRYSTAL ; PROJECT; PROTECT; CIRCUIT; TFT; PAIR; CONNECT; RESISTOR; DIVIDE; DIVIDE ; VOLTAGE; SET; LEVEL; ONE; DIRECTION; OVERVOLTAGE; APPLY

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**File Segment:** EPI; EngPI

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**ELECTROOPTICAL DEVICE**

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**ABSTRACT**

**PURPOSE:** To enhance the reliability of the display device for which an electrooptical element, such as liquid crystal, is utilized or the device which applies this device and for which device thin-film transistors(TFTRs) are used and to prolong the life of the device by proposing the device which prevents the destruction of the TFTRs by the surge voltage infiltrated from the outside by a certain cause.

**CONSTITUTION:** The two TFTRs of a p channel type and n channel type are formed on a transparent substrate consisting of glass, etc., and gate electrodes 1303 and source and drain electrodes 1304, 1305 thereof are connected by wirings 1307, 1308 to be used as resistors, by which the circuit necessary as a protective circuit is constituted. This protective circuit is produced by the same stage as for the stage for producing the TFTRs of the p channel type or n channel type or both thereof formed in display element regions.